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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/752,503	01/08/2004	Masaru Kito	04329.3220	5634

7590 11/03/2004

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EXAMINER	
WILSON, SCOTT R	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 11/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/752,503	KITO ET AL.	
	Examiner	Art Unit	
	Scott R. Wilson	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 September 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) *9-16* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/8/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Applicant's election without traverse of claims 1-8 in response filed 24 September 2004 is acknowledged.

Drawings

Figure 17 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.121(d)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1 and 3-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsai et al. in view of Shiho et al.. As to claim 1, Tsai et al., Figure 3K, discloses a trench capacitor comprising a semiconductor substrate (300), a trench, formed in the semiconductor substrate having upper (372) and lower (370) portions, a first doped polysilicon layer (370) filled in the lower portion through a first dielectric film (360') and doped with a first impurity having a first conductivity type (col. 3, lines 55-58), a second doped polysilicon layer (372) filled in the upper portion through a second dielectric film (380') and doped

with a second impurity different from the first impurity (col. 4, lines 10-12), the second impurity having the first conductivity type. Tsai et al. discloses two possible dopants, one of which may be doped in the lower portion (370), and the other of which may be doped in the upper portion (372). Tsai et al. does not disclose expressly a buried strap layer provided on the second doped polysilicon layer and composed of the first doped polysilicon layer. Shiho et al., Figure 7, discloses a trench capacitor formed with a buried strap layer (30), which is composed of doped polysilicon (col. 5, lines 52-53). At the time of invention, it would have been obvious to a person of ordinary skill in the art to form the strap layer of Shiho et al. in the capacitor of Tsai et al.. The motivation for doing so would have been to form a capacitor which could be used in a DRAM. Therefore, it would have been obvious to combine Shiho et al. with Tsai et al. to obtain the invention as specified in claim 1.

Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tsai et al. in view of Shiho et al. and further in view of Nitayama et al.. Tsai et al. in view of Shiho et al. discloses the invention of claim 1, as described above. Tsai et al. in view of Shiho et al. does not disclose expressly a third doped polysilicon layer formed between the first doped polysilicon layer and the second doped polysilicon layer. Nitayama et al., Figure 4B, discloses a trench capacitor formed with three doped polysilicon layers (120), (124) and (112). At the time of invention, it would have been obvious to a person of ordinary skill in the art to form a third doped polysilicon layer, akin to that of Nitayama et al., between the two doped polysilicon layers of Tsai et al.. The motivation for doing so would have been to form a capacitor which would have the same range of capacitance as that of Nitayama et al.. Therefore, it would have been obvious to combine Shiho et al. and Tsai et al. with Nitayama et al. to obtain the invention as specified in claim 2.

As to claim 3, Tsai et al. discloses (col. 3, lines 55-58) and (col. 4, lines 10-12) that the first impurity may be arsenic and that the second impurity may be phosphorus.

As to claim 4, Tsai et al. discloses (col. 4, lines 60-62) that the impurity concentration of the second doped polysilicon layer is varied around a value centered at 5×10^{20} per cm^3.

As to claim 5, Tsai et al. discloses (col. 3, line 58) that the thickness of the first doped polysilicon region (370) varies from 200 nm to 300 nm, which necessarily implies that the thickness of the second doped polysilicon region (372) varies in thickness over a range of 100 nm.

As to claim 6, Tsai et al., Figure 3K, discloses that the film thickness of an upper portion of the second dielectric film (371') is thinner than that of a lower portion (360') thereof.

As to claim 7, Tsai et al., Figure 3K, discloses that the second doped polysilicon layer (372) is formed at the upper portion of the second dielectric film (371').

As to claim 8, Shiho et al., Figure 15, discloses that the buried strap layer (30) is positioned at the upper portion of the second dielectric film (26), which would correspond to the dielectric film (380') and (371') of Tsai et al.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Scott R. Wilson whose telephone number is 571-272-1925. The examiner can normally be reached on M-F 8:30 - 4:30 Eastern.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

srw
October 21, 2004